REMARKS/ARGUMENTS

Claims 1 and 4 are pending in this Application. By this amendment, Applicant has amended claims 1 and 4.

Claims 1 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Miyauchi (U.S. Patent No. 5,717,886). Applicant respectfully traverses the rejection of claims 1 and 4.

Claim 1 recites:

> "A data processing device comprising:
> a read-only memory;
> a flash memory capable of modifying information stored therein and adding information thereto;
> a central processing unit performing data processing using information stored in said read-only memory and said flash memory;
> an information storage area provided in said flash memory for storing predetermined modifiable information among the information used by said central processing unit for data processing;
> an address storage area provided in said flash memory for storing at least the address of the information stored in said information storage area; and
> an address-modification control unit for, after at least one of modification of modifiable information stored in said information storage area and addition of modifiable information to said information storage area, and in accordance with said one of the modification of the information and addition of the information, performing one of modification of the address of the information stored in said address storage area and addition of the address of the information to said address storage area; wherein
> the information used by said central processing unit for data processing can be freely modified or added; and
> **the address-modification control unit controls a function address table area including at least one address of a subroutine program used in a main program executable by the central processing unit for performing data processing and a variable address table area including at least one address of a variable used in the main program.**" (emphasis added)

Claim 4 recites:

"A method in a data processing device comprising:
a read-only memory;
a flash memory capable of modifying information stored therein and adding information thereto;
a central processing unit performing data processing using information stored in said read-only memory and said flash memory;
an information storage area in said flash memory; and
an address storage area in said flash memory;
said method comprising the steps of:
storing in said information storage area predetermined modifiable information among the information used by said central processing unit for data processing;
storing in said address storage area at least the address of the information stored in said information storage area;
performing at least one of modification of modifiable information stored in said information storage area and addition of modifiable information to said information storage area; and
then, in accordance with said one of modification of the information and addition of the information, performing one of modification of the address of the information, stored in said address storage area and addition of the address of the information to said address storage area; wherein
the information used by said central processing unit for data processing can be freely modified or added; and
the address storage area includes a function address table area including at least one address of a subroutine program used in a main program executable by the central processing unit for performing data processing and a variable address table area including at least one address of a variable used in the main program." (emphasis added)

Applicant's claim 1 recites the feature of "the address-modification control unit controls a function address table area including at least one address of a subroutine program used in a main program executable by the central processing unit for performing data processing and a variable address table area including at least one address of a variable used in the main program." Applicant's claim 4 recites the feature

of "the address storage area includes a function address table area including at least one address of a subroutine program used in a main program executable by the central processing unit for performing data processing and a variable address table area including at least one address of a variable used in the main program." With the improved features of claims 1 and 4, Applicant has been able to provide a data processing device in which the main program and information regarding functions can be freely modified (see, for example, the fourth full paragraph on page 2 of the originally filed Specification), and more specifically, the functions or subroutines used by the main program to perform data processing and the variables used by the main program for data processing can be freely modified (see, for example, the first full paragraph on page 4 of the originally filed Specification).

In the Advisory Action dated June 25, 2004, the Examiner alleged "prior art still renders claims unpatentable and the final rejection is deemed to be proper with respect to applicant's arguments filed 4/19/04. Claim 1, lines 20-21 and claim 4, lines 24-25 do not recite what information [is] stored in the 'function address table area' and the 'variable address table area.' Miyauchi shows a function address table area (e.g., figs. 20-21, LSA table of flash memory 104, which performs a function of storing addresses or table 103 which performs a function of converting addresses; col. 3, lines 45-65; or figs. 6-7 a directory table of flash memory 104a performing a function of storing a starting address A wherein file A has DAT function; col. 8, lines 5-10 and 15-35) and a variable address table area (e.g., figs. 20-21, LSA-PSA table 103 storing relationships LSA and PSA which tends to vary or LSA table of the flash memory 104 storing an address wherein the address or data of the address tends to vary; col. 3, lines 45-65; col. 2, lines 40-50; or figs. 6-7 a directory table of flash memory 104a having variable fields and for storing an address of data which tends to vary; col. 8, lines 25-35; and col. 10, lines 45-60) or Miyauchi shows the address storage area includes a function address table area (e.g., figs. 20-21, a first LSA table of flash memory 104, which performs a function of storing addresses; col. 3, lines 45-65; or figs. 6-7 a directory table

of flash memory 104a, which performs a function of storing a starting address A wherein file A has DAT function; col. 8, lines 5-10 and 15-35) and a variable address table area (e.g., figs. 20-21, a second LSA table of flash memory 104, which stores an address wherein the address or data of the address tends to vary; col. 3, lines 45-65; col. 2, lines 40-50; or figs. 6-7 a directory table of flash memory 104a having variable fields and for storing an address of data which tends to vary; col. 8, liens 25-35; and col. 10, lines 45-60) as claimed."

Applicant has amended claims 1 and 4 to recite "the address-modification control unit controls a function address table area **including at least one address of a subroutine program used in a main program executable by the central processing unit for performing data processing** and a variable address table area **including at least one address of a variable used in the main program**," (emphasis added) respectively.

The Examiner alleged that Miyauchi teaches an LSA table "which performs a **function** of storing addresses," a table 103 "which performs a **function** of converting addresses," a directory table of flash memory 104a which performs "a **function** of storing a starting address," "LSA-PSA table 103 storing relationships LSA and PSA which **tend to vary**," and "a directory table of flash memory 104a having **variable fields** and for storing an address of data which **tends to vary**."

The Examiner has improperly alleged that the "function" and "variable" aspects of Miyauchi highlighted by the Examiner somehow constitute the claimed function address table area and the variable address table area. However, the alleged "function" of Miyauchi is merely a "function" or operation that is actually performed to store or convert addresses of data, and is clearly not a subroutine program used in a main program executable by the central processing unit for performing data processing. Further, Miyauchi does not teach anything about an area for storing an address of such a subroutine or function. In addition, the "vary" or "variable fields" aspects of Miyauchi highlighted by the Examiner and the alleged "variable" of Miyauchi are clearly not a

variable used in the main program to perform data processing. Also, Miyauchi clearly fails to teach anything at all about an address of a variable used with a main program for performing data processing.

Absolutely none of the elements of Miyauchi cited by the Examiner teaches or suggests includes a function address table area **including at least one address of a subroutine program used in a main program executable by the central processing unit for performing data processing** and a variable address table area **including at least one address of a variable used in the main program**. In fact, Miyauchi fails to teach or suggest **any** elements which include any storage address for a function or subroutine or variables used in a main program executable by a central processing unit to perform data processing.

In contrast to the present claimed invention, Miyauchi is directed to a device for determining conversion between **Logic Sector** Addresses (LSA) and **Physical Sector** Address (PSA) for data that is stored in the flash memory **104**. **All** of the data of Miyauchi has two addresses associated therewith, an LSA and an PSA. The LSA is a logic sector address of a host unit, and the PSA is the physical sector address of a disk unit. Miyauchi teaches converting between LSA and PSA for tracking data stored in the temporary memory of a computer.

Miyauchi clearly fails to teach or suggest **ANY** elements which store functions or subroutines, which are used by a main program that is executable by a central processing unit to perform data processing, in a totally separate area from a storage area for variables used by the main program that is executable by a central processing unit to perform data processing.

Further, there is no disclosure or suggestion in Miyauchi that the address of any of the information stored on the semiconductor disk device **100** is segregated into a function address table area including at least one address of a subroutine used by a main program that is executable by a central processing unit to perform data processing, and a variable address table area including at least one address of a

variable used by the main program to perform data processing.

Thus, the LSA-PSA conversion table of Miyauchi clearly fails to teach or suggest anything at all relating to a function address table area including at least one address of a subroutine program used in a main program executable by the central processing unit for performing data processing and a variable address table area including at least one address of a variable used in the main program as recited in Applicant's claims 1 and 4.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 and 4 under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Miyauchi.

Accordingly, Applicant respectfully submits that AAPA and Miyauchi, applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements and method steps recited in claims 1 and 4 of the present application.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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